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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/368,918	08/05/1999	RICHARD L. TRABER	3COM-2200.IP	6088

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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	PAPER NUMBER
2133	3

DATE MAILED: 04/10/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/368,918	TRABER ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☒ Claim(s) *4 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

Corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance (see attached PTO-948).

Claim Objections

Claims 4 and 15 are objected to because of the following informalities: "an stage progression signal" in lines 11-12 needs to be corrected so that it is written in correct Idiomatic English. Claim 15 cites the same language in line 6 of claim 15. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner would like to point out that the phrase "during a first stage" in line 5 of claim 4 is indefinite since one of ordinary skill in the art at the time of the invention would understand "first stage" to refer to a sequential circuit whereas the term "during"

implies that the applicant is trying to use "first stage" in another context contrary to what one of ordinary skill in the art at the time of the invention would understand.

The Examiner would like to point out that the phrase "during a second stage" in line 8 of claim 4 is indefinite since one of ordinary skill in the art at the time of the invention would understand "second stage" to refer to a sequential circuit whereas the term "during" implies that the applicant is trying to use "second stage" in another context contrary to what one of ordinary skill in the art at the time of the invention would understand.

While applicant may be his or her own lexicographer, a term in a claim may not be given a meaning repugnant to the usual meaning of that term. See *In re Hill*, 161 F.2d 367, 73 USPQ 482 (CCPA 1947). The terms "first stage" and "second stage" in claim 4 are used by the claim to mean "steps of some sort of algorithm", while the accepted meaning is "a sequential circuit or a stage within a sequential circuit".

Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: a definition of a step that would lead to the statement "during a first stage" (activity).

Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See

MPEP § 2172.01. The omitted steps are: a definition of a step that would lead to the statement "during a second stage" (activity).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Steele, Randy C. (US 5299203 A).

Steele teaches:

"An integrated circuit having a normal operating mode and a special operating mode, such as a special test mode, is disclosed. The **special test mode is enabled by a series of signals**, such as overvoltage excursions at a terminal, rather than by a single such excursion, so that it is less likely that the special test mode is entered inadvertently, such as due to noise or power-down and power-up of the device. The **circuit for enabling the test mode includes a series of D-type flip-flops**, each of which are **clocked upon detection of the overvoltage condition** together with a particular logic level applied at another terminal; **multiple series of flip-flops** may be provided for multiple special test modes" (see Abstract, Steele);

"An example of a **special test mode** is an internal "parallel", or multi-bit, test mode. Conventional parallel test modes allow access to more than one memory location in a single cycle, with common data written to and read from the multiple locations simultaneously. For memories, which have **multiple input/output terminals**, multiple bits would be accessed in such a mode for each of the input/output terminals, in order to achieve the parallel test operation. This parallel test mode of course is not available in normal operation, since the user must be able to independently access each bit in order to utilize the full capacity of the memory. Such parallel testing is preferably done in such a way so that the multiple bits accessed in each cycle are physically separated from one another, so that there is little likelihood of pattern sensitivity interaction among the simultaneously accessed bits. A description of such parallel testing may be found in McAdams et al., "A 1-Mbit CMOS Dynamic RAM With Design-For-Test Functions",

IEEE Journal of Solid-State Circuits, Vol SC-21, No. 5 (October 1986), pp. 635-642."(col. 2, lines 3-23, Steele);

"**Test mode enable circuitry 29**, as noted above, receives signals on lines A1, A3, and TRST as inputs. Test mode enable circuitry 29 presents signals on line T to parallel test circuitry 28, as noted above, to **indicate whether or not the parallel test mode is enabled**. Additionally, test mode enable circuitry 29 has another output on line T2, for enabling a second special test in memory 1, if desired. Line T2 is connected to such other circuitry in memory 1 as is necessary for performing such an additional test; such other special test, in this embodiment, is mutually exclusive with the parallel test function indicated by the signal on line T. While only two mutually exclusive **special test modes** are shown on FIG. 2, it is of course contemplated that many more special test functions may be enabled by simple extension of the logic included in test mode enable circuitry 29, including the use of additional ones of inputs such as address inputs for the selection of such additional special test modes. It is contemplated that such extension will be apparent to one of ordinary skill in the art having reference to this specification. Furthermore, it should be noted that the special test modes enabled by test mode enable circuitry 29 need not be mutually exclusive of one another, as certain functions may work cooperatively with one another (e.g., a particular special read function may be enabled together with the parallel test mode, with the parallel test without the special read function separately selectable)." (col. 9, lines 30-57, Steele);

"Further included in test mode enable circuitry 29 is **power-on reset circuit 40**, which provides an enable signal on line POR to evaluation logic 30 (as well as to other circuitry in memory 1) at a point in time after power supply V_{cc} is powered up. As will be described in further detail hereinbelow, power-on reset circuit 40, via evaluation logic 30, will lock out entry into test mode during power-up of memory 1" (col. 10, lines 5-12, Steele); and

"Node N1 is connected to the input of a conventional inverting **Schmitt trigger circuit 40**. As is conventional for such circuits, **Schmitt trigger 40** performs the logical inversion with hysteresis in its transfer characteristic. Such hysteresis, provided by n-channel transistor 42_n and p-channel transistor 42_p, provides stability to overvoltage detector 32, so that small variations in the voltage of line A3 around the trip voltage will not cause the output of overvoltage detector 32 to oscillate between high and low logic levels."(col. 11, lines 19-28, Steele).

The Examiner would like to point out that the circuit depicted in Figure 2 of Steele is a test enable assertion system comprising a power-on reset Schmitt trigger circuit for use in asserting various special test modes coupled to a series of clocked flip-flops, (i.e., a

staging component) for advancing logical values of said trigger signal in response to a clock signal (i.e., a progression signal).

However Steele does not explicitly teach that the switch is for use in an automatic scan test.

The Examiner would like to point out that the test enable circuit of Steele is based on sequential logic which clearly suggests the use of the test enable circuit of Steele in an automatic scan test.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Steele by including use for the switch in an automatic scan test.

This modification would have been obvious to one of ordinary skill in the art, at the time of the invention, because one of ordinary skill in the art at the time of the invention would have recognized that use of the switch in an automatic scan test would provide the opportunity to improve fault tolerance in system applications requiring error-free data.

Claims 2-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steele, Randy C. (US 5299203 A).

Steele teaches the additional limitations of claim 2. Use of PCI reset and clock-signals does not deviate from the scope or the intent of the teachings of Steele.

Steele teaches the additional limitations of claim 3. See rejection to claim 1, above. The examiner would like to point out that the test enable circuitry in Steele is responsive to the TRST signal, which is responsive to inputs E1 and E2 in Figure 1 of Steele, which clearly suggests use of a tester for controlling the test enable circuitry in Steele.

Steele teaches the additional limitations of claims 4 and 6. See Figures 2 and 5b in Steele.

Steele teaches the additional limitations of claim 5. Use of PCI reset and clock-signals does not deviate from the scope or the intent of the teachings of Steele.

Steele teaches the additional limitations of claims 7 and 8. Use of a specific value for the trigger signal does not deviate from the scope or the intent of the teachings of Steele.

Steele teaches the additional limitations of claim 9. Use of a test vector to initiate a test would have been well known to those of ordinary skill in the art in the art at the time of the invention (for example, see Prior Art admission on page 3, 2nd paragraph of the Applicant's specification).

Steele teaches the additional limitations of claim 10. Use of a network card does not deviate from the scope or the intent of the teachings of Steele.

Steele teaches the additional limitations of claim 11. See rejection to claim 1, above. In addition, Figure 1 of Steele is substantially a test enable activation system with a functional component (Memory Array 10) and Input/output circuitry 16. The Examiner would like to point out that Input/output circuitry 16 is coupled to test enable circuitry 29 through OR gate 22 and, the fact that output 20 is only wide enough for one word at a time clearly suggests multiplexing capabilities for the Input/output circuitry 16. The Examiner would also like to point out that a particular implementation of the circuit in Steele using an MUX and a NAND gate does not deviate from the scope or the intent of the teachings of Steele.

Steele teaches the additional limitations of claim 12-14. The Examiner would like to point out that a particular implementation of Input/output circuitry 16 would not deviate form the scope or the intent of the teachings of Steele.

Steele teaches the additional limitations of claim 15-21. See rejection to claim 1, above. In addition, See Figures 6-9 in Steele.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kahn, Michael F. et al. (US 5167020 A) teaches a data transmitter with dual buffers operating separately and having scan and self-test modes.

Sprouse, Jeffrey A. et al. (US 5951703 A) teaches functionally scan testing a digital system. Pressly, Matthew D. et al. (US 5889788 A) teaches speed path testing of conductive paths in an integrated circuit containing an embedded core. James, David B. (US 5768289 A) teaches a method and apparatus for generating test and programming signals on a printed circuit board. Bradford, William F. et al. (US 5726999 A) teaches a method and apparatus for universal programmable boundary scan driver/sensor circuit. Sukegawa, Shunichi et al. (US 5596537 A) teaches a test circuit for initiating the execution of a testing procedure with respect to a semiconductor device. Bui, Cuong M. (US 5479127 A) teaches a circuit that generates a self-resetting bypass control. Bianco, Mark E. et al. (US 5357572 A) teaches an apparatus and method for sensitive circuit protection with set-scan testing. Levy, Paul S. US (5130645 A) teaches a built-in self-test structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Joseph D. Torres, Ph.D.
Art Unit 2133
March 13, 2002

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